REMARKS

It is believed that this Amendment is fully responsive to the Office Action dated **April 21, 2004**.

Allowable Subject Matter

Claims 1-9 are allowed. Apparently the Examiner is not aware that claims 13-14 and 18-21 are directly or indirectly dependent upon allowed claim 1. Therefore, claims 13-14 and 18-21 should also be allowed by virtue of their dependence upon an allowed independent claim. Allowance of claims 13-14 and 18-21 is respectfully requested.

Claim Rejections under 35 USC §103

Claims 10 and 15 are rejected under 35 USC §103(a) as being unpatentable over Okid (JP P2000-183224 A) in view of Okoshi et al. (U.S. Patent No. 5,665,473).

The present invention is a semiconductor device (1) as shown in Figure 3. This semiconductor device (1) includes a metal plate (stiffener 12), and a wiring substrate (10) having an insulating substrate (insulating film 16), a signal wiring layer (20) formed on one surface of the insulating substrate (insulating film 16), and a ground plane (18) formed on another surface of the insulating substrate (insulating film 16). As shown in Figure 4, the signal wiring layer (20) is made of a wiring line portion (20a) and a connection pad portion (20b) whose width is thicker than a width of the wiring line portion (20a). As shown in Figure 3, a non-forming portion (18a) is provided in portion of the ground plane (18), which corresponds to the connection pad portion

(20b). In addition, a recess portion (12a) may be formed in portion of the metal plate (stiffener 12), which correspond to the non-forming portion (18a). The recess portion (12a) of the metal plate (stiffener 12) is formed as a hollow, or is filled with a resin layer.

Okid describes in the English Translation Abstract a semiconductor device and a wiring board (101) formed on a substrate (101A). A solder bump (108A-108D) is also shown.

Okoshi et al. describes a package for mounting a semiconductor device in which the base plate (4) is made of ceramic or metal.

The invention of claim 10 relates to a semiconductor package, and is characterized to comprise a metal plate, and a wiring substrate including an insulating substrate and a signal wiring layer formed on a one surface of the insulating substrate, the wiring .substrate whose another surface is adhered onto the metal plate, wherein the signal wiring layer is constructed by a wiring line portion and a connection pad portion whose width is thicker than a width of the wiring line portion, and a recess portion is provided in a portion of the metal plate, which corresponds to the connection pad portions.

In claim 10, in order to attain the impedance matching between the wiring line portion of the signal wiring layer and the connection pad portion whose width is larger than that of the wiring line portion, the recess portion is provided in a portion of the metal plate, which corresponds to the connection pad portions.

And, in the invention claim 15, the wiring substrate is a film substrate, wherein stress applied to the bump is relaxed by providing a recess portion in a portion of the metal plate, which corresponds to the connection pad portion.

The examiner points out that Okid shows a structure of a semiconductor device, comprising a substrate 101A, and a wiring substrate including a film substrate, and a signal wiring layer having a connection pad portion which is joined to a bump 108A, the film substrate whose another surface is adhered onto the substrate 101A, wherein stress applied to the bumps is relaxed by providing a recess portion in a portion of the substrate.

However, it is not described in Okid that a recess portion is provided a portion of the substrate 101A which corresponds to the connection pad portions in order to attain the impedance matching. In order to demonstrate this point, a translation of Okid is attached to this Request for Reconsideration which is translated by computer.

It is only described in Okid that in order to prevent the generation of the electrical short of mutual metallic thin wires for connecting the electrode of the semiconductor chip with the wiring of a substrate, the annular wiring 104 for a power source is arranged closer to a semiconductor chip 114 than the post-shaped wiring 103 for a signal, and the post-shaped wiring 103 for a signal is arranged higher than the annular wiring 104 for a power source.

That is, in Okid, since to attain the impedance matching in wiring substrate 101A is not described at all, there is no inevitability of providing the recess in the substrate 101 A.

Also, it is not described in Okid that stress applied to the bump is relaxed by providing a recess portion in a portion of the substrate 101A.

In addition, in Okoshi, it is only described that base plate 4 is formed of a ceramic or a metal, constitutions of claims 10 and 15 is not describe at all.

In order to facilitate the Examiner's understanding a translation of Okid is attached to this Request for Reconsideration.

Therefore, withdrawal of the rejection of Claims 10 and 15 under 35 USC §103(a) as being unpatentable over Okid (JP P2000-183224 A) in view of Okoshi et al. (U.S. Patent No. 5,665,473) is respectfully requested.

Conclusion

In view of the aforementioned remarks, the claims are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

George N. Stevens
Attorney for Applicant
Reg. No. 36,938

GNS/alw
Atty. Docket No. **030942**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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PATENT TRADEMARK OFFICE

Enclosure: Translation of Okid

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